PUBLIC DISCLOSURE

Centre for OSAT

National Institute of Technical Teachers' Training and Research (NITTTR), Bhopal

1. Introduction

The Centre for OSAT (Outsourced Semiconductor Assembly and Test) at NITTTR Bhopal focus on semiconductor packaging and testing, which form a critical stage in the semiconductor manufacturing value chain. Semiconductor packaging connects silicon chips to external electronic systems while ensuring electrical connectivity, protection, and reliability. With the rapid growth of electronics applications such as smartphones, cloud computing, IoT devices, and electric vehicles, global demand for semiconductor chips has increased significantly. India currently imports a large share of its semiconductor requirements, and national initiatives such as the India Semiconductor Mission (ISM) and Semicon India Program aim to develop indigenous capabilities in semiconductor design, manufacturing, assembly, and testing. In alignment with these initiatives, the OSAT facility at NITTTR Bhopal contributes to skill development, innovation, and research in semiconductor packaging technologies.

The OSAT laboratory has been established to create a basic semiconductor assembly and packaging facility and to conduct skilling and training activities for students, researchers, and faculty members from engineering colleges, polytechnics, and universities. The facility supports hands-on training for UG, PG, and PhD students, faculty development programs, including Diploma in Semiconductor Packaging (OSAT/ATMP). In the last two years, more than 800 students and faculty members from various academic institutions have visited the OSAT Centre for laboratory exposure, internships, and training programs. The centre also offers customized and targeted training programs for academia and industry, helping bridge the skill gap in semiconductor assembly and test operations.

The OSAT facilities at NITTTR is equipped to design and development of Semiconductor devices packages such as Power MOSFET, Triode, Diode, MESFET, IGFET, SCR, Sensors (Pressure, Temperature, Accelerometer, Gas Sensor), Photo-diodes, MEMS devices, Zener diode, Optoelectronic devices and ISFET. Package design classification are Ball Grid, QFN, TO (TO-03, TO-05), LGA, QFP, CSP, WLSP and DIP. The technologies are Advanced 2.5D/3D hetero packages.

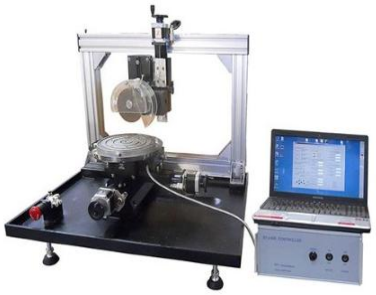
With the rapid growth of the semiconductor sector in India, there is an increasing need for skilled manpower in semiconductor assembly, packaging, and testing technologies. The facility at NITTTR Bhopal aims to support this national requirement by providing hands-on training, research opportunities, prototype development, and industry collaboration.

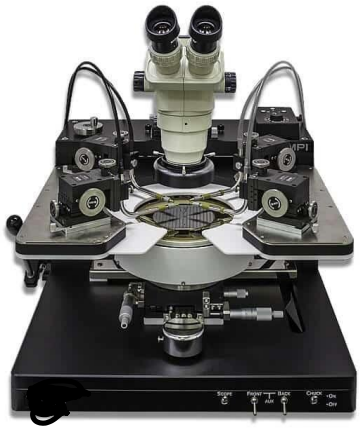
The lab supports:

- Training in semiconductor packaging processes
- Development of indigenous testing and packaging equipment
- Hands-on exposure to chip assembly and reliability testing

2. Major Equipment and Facilities Available

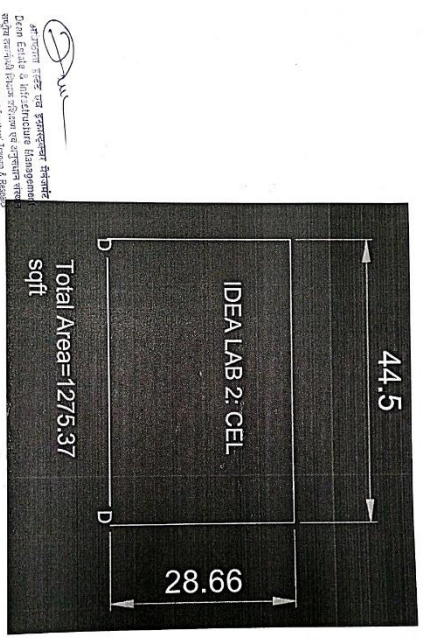
The OSAT facility is equipped with specialized equipment for semiconductor device assembly, testing, and prototype development. ***(pictures attached in the end of report)***

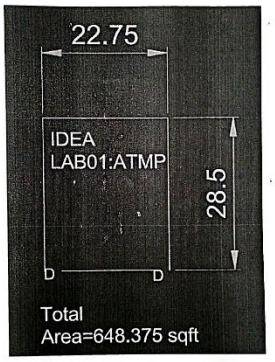
S. No.	Equipment	Approx. Cost	Photograph
1	Die Bonder	₹41,89,000	
2	Wire Bonder	—	
3	Wafer Dicing Machine	₹29,84,400	
4	High Temperature Furnace	₹79,882	
5	Laboratory Ovens (2 units)	₹58,000	

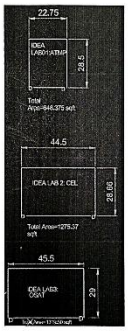
S. No.	Equipment	Approx. Cost	Photograph
6	Probe Station	₹4,48,400	
7	3D Printer	₹1,20,000	
8	Laminar Flow Units (4 units)	—	
9	Semi-Automatic Screen Printer	₹3,49,000	
10	Chemical Fume Hood	₹2,08,110	

These facilities enable the laboratory to perform semiconductor die preparation, chip assembly, interconnection, and testing activities.

3. Physical Layout of OSAT & ATMP Labs at NITTTR Bhopal:







4. Utilisation of the OSAT Facility

The OSAT facility is used for education, research, skill development, and prototype fabrication in semiconductor technology.

Semiconductor Assembly

- Wafer dicing into individual semiconductor dies
- Die attachment onto substrates
- Wire bonding for electrical interconnections

Device Characterization

- Electrical probing of semiconductor devices
- Thermal testing and reliability preparation

Prototype Development

- Development of packaging solutions for electronic devices
- Sensor and MEMS device packaging

Academic Training

- Laboratory training for Diploma, UG, PG and PhD students, Internship and Apprentices
- Demonstrations for faculty development programs
- Hands-on training in semiconductor assembly processes

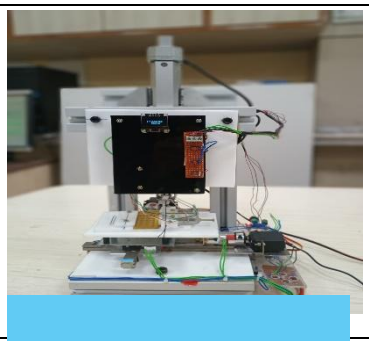
4. Indigenous Equipment Development

One of the major objectives of the OSAT Lab is to develop indigenous semiconductor equipment to reduce dependency on imported systems and to promote innovation in semiconductor manufacturing.

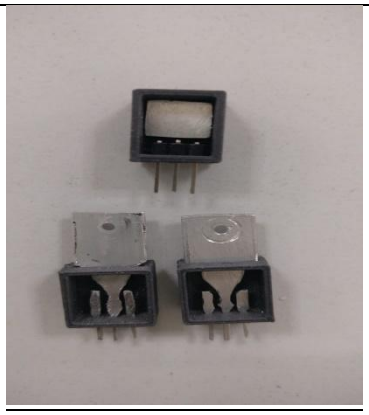
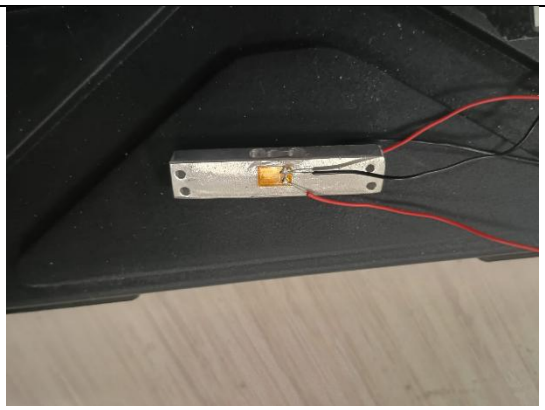
4.1 In-House Wafer Dicing Machine

Developed an indigenous system capable of precision cutting of semiconductor wafers into individual dies. Impact: • Reduced dependence on imported semiconductor machines • Provided hands-on exposure to precision mechanical design and automation systems • Demonstrated capability for indigenous semiconductor equipment development	

4.2 Indigenous Bond Pull Tester

Development of a system capable of measuring bond strength of wire bonds in semiconductor devices. Importance: Bond pull testing is an essential quality control procedure in semiconductor packaging, ensuring the reliability of microelectronic connections.	

4. Semiconductor Packaging Projects

5.1 Power MOSFET Packaging OSAT has initiated projects involving packaging of power semiconductor devices i.e. Power MOSFET, including: • Die attachment • Wire bonding • Electrical testing These projects provide practical exposure to power electronics packaging technologies used in industrial applications.	
5.2 Load Cell Chip Packaging In this project, specialized semiconductor chips are mounted on aluminium load cells for sensing applications. Innovation: • Precise alignment of silicon dies • Bonding onto metallic substrates • Integration of semiconductor sensing elements with mechanical structures	

6. Process Optimization

To improve packaging efficiency, students at OSAT Lab is working on batch processing techniques. Multi-Chip Processing Using Custom Jigs: Currently, semiconductor chips are processed individually. The lab is developing custom jigs to enable simultaneous processing of multiple chips.

Expected Benefits:

- Increased production throughput
- Transition from lab-scale processing to pilot-scale manufacturing
- Demonstration of design for manufacturability

7. Training and Outreach Activities:

7.1: Students from Schools, Colleges and faculty members from many states visited OSAT Facilities.

Activities:

- Laboratory tours
- Semiconductor technology demonstrations
- Interaction with researchers and faculty

These visits promote scientific curiosity and innovation among school and College students.

7.2 Internships/Apprenticeship Program on Semiconductor Packaging

Short term/ long term Internships and apprenticeship has been carried out at OSAT.

Training Topics

- Semiconductor manufacturing overview
- Packaging materials
- Assembly techniques
- Reliability testing methods

Participants gained hands-on exposure to semiconductor packaging workflows.

8. Industry Contribution & MoU:

Industry and Academia collaboration plays an important role in strengthening OSAT activities at NITTTR Bhopal. MoUs have been signed with Many Industries and Academic Institutions.

S.No	Name of Institute/Industry	Logo
1	Suchi Semicon Pvt. Ltd, Surat, Gujarat	
2	CEERI Pilani	
3	NIT Raipur	
4	IIT Mandi	

5	NIT Patna	
6	Cotton University, Assam	

Nature of Contribution

Industry partners support the lab through:

- Sponsoring innovation projects
- Providing engineering guidance
- Supporting development of indigenous equipment
- Mentoring students and faculty

This collaboration ensures that OSAT lab projects remain aligned with real industrial requirements and technological trends.

9. Personnel:

S. No.	Name of Position	Details
1.	Chief Mentor	Prof. C. C. Tripathi Director, NITTTR, Bhopal Email: director@nitttrbpl.ac.in Contact No.:9416280555
2.	HoD, DEEE	Prof. A. S. Walkey Email:aswalkey@nitttrbpl.ac.in Contact No.:8989792155
3.	Chief Technical Officer (CTO, OSAT)	Dr. P. K. Khanna Email: pkkhanna@nitttrbpl.ac.in Contact No.:9829331122
4.	OSAT Coordinator	Dr. Pallavee Bhatnagar (Professor) Email:pbhatnagar@nitttrbpl.ac.in Contact:9826233040
5.	Coordinator (PG in VLSI & Microelectronics, Diploma in Semiconductor Packaging (OSAT/ATMP))	Dr. Seema Verma (Professor) Email:sverma@nitttrbpl.ac.in Contact:9950786677
6.	Co-Coordinator (Diploma in Semiconductor Packaging (OSAT/ATMP)	Dr. Shilpi (Assistant Professor) Email: shilpi.nitj@gmail.com Contact:9466229362
7.	Post Doc Fellow	Vacant
8.	Technical Manpower	Mr. Akhil Mr. Ravi Kumar Mr. Rakesh Shamra
9.	Interns' Capacity/Seats	10

10. Fee Structure:

Title	Duration/Fee
Internship	• Internship fee Rs. 3000/- may be charged for internship/training in OSAT for two weeks/40 hrs. • Summer Training Certificate Courses (4 to 6 weeks/ 80 hours) for Students of AICTE approved institutes: 6,000/- + GST @ 18%

	• Customized Courses for Industry Personnel (1 to 2 weeks/ 40 hours) 10,000/- + GST @ 18% • Advanced Certificate Courses for Students (about 12 weeks or 3 months/ 240 hours): 12,000/- + GST @ 18% • Project / Dissertation work (6 months duration) 15,000/- + GST @ 18% • One Year training (Post B.Tech) in relevant Branch: 18,000/- + GST @ 18%
Diploma in Semiconductor Packaging (OSAT/ATMP)	Rs. 36,000/- for 06 Months/06 Module (Rs. 6000/- per module)

11. Publications & IPR:

Patent

1. **Shilpi**, Ravi Prasad, P. K. Khanna, A.S. Walkey and C. C. Tripathi, "*A Process for Customized Packaging of Semiconductor Devices*" Indian Patent Application No. 202521114810, Filed on 21st November, 2025.

Conferences

1. **Shilpi**, Ravi Prasad, P. K. Khanna and C. C. Tripathi, "*Packaging Strategy and OSAT Processes for Discrete Power MOSFET Devices: A Concise Review*," National Conference on Emerging Micro/Nano-Electronics: Devices, Technology & VLSI Design (EMNE - 2024), Kurukshetra, India, 7th to 8th Nov, 2024.

2. **Shilpi**, Ravi Prasad, P.K. Khanna and C. C. Tripathi, "*Multi-Chip Module Design for Versatile RC Active Filters with Stacked Chip Components*," International Conference on Semiconductor Technologies – Materials To Chips (ICST - 2024), Noida, India, 18th to 20th September, 2024, p. 190.

11. Benefits and Impact

Educational Impact

- Provides hands-on training in semiconductor packaging technologies
- Supports UG, PG, and PhD research projects

Research Impact

- Development of indigenous semiconductor equipment
- Innovation in semiconductor packaging and reliability testing

Industrial Impact

- Collaboration with electronics and semiconductor industries
- Development of prototype packaging solutions for industry

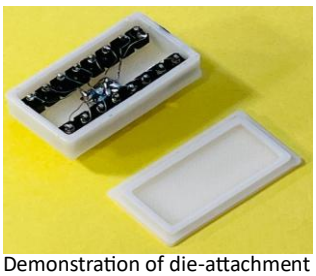
National Impact

- Contributes to skill development in semiconductor manufacturing
- Supports India's growing semiconductor ecosystem

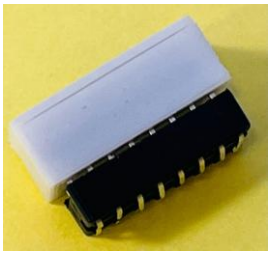
Packages developed for Semiconductor Device Packaging at OSAT Lab., NITTTR, Bhopal

Batch production of 16 pin DIP packages

Package (inner view)



Demonstration of die-attachment



Package (attached to connector)

Package developed for Industry